Space: The Final Frontier – FPGAs for Space and Harsh Environments

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The last 20 years have seen the explosion of FPGA technology used in many different end applications, including those within harsh environments. It therefore follows that system developers wish these devices to operate correctly and safely regardless of environment. When engineers design for a spaceflight mission, there are three main environmental factors that will impact performance: radiation; temperature; and vibration and shock.

Of course, the type of spaceflight mission will impact to what degree these factors need to be considered. For a launcher, for example, vibration and shock are perhaps more critical than the total radiation dose the launcher will encounter during its brief lifetime. For this reason, when talking about spaceflight there are four major classes of mission to consider, each with typical orbits and lifetimes (which is not to say those lifetimes will not be extended).

1. Launcher – typical lifetime less than 20,000 seconds
2. Telecommunications – 17-year operating life, geosynchronous orbit
3. Science – Seven-year interplanetary mission, e.g. Solar Orbiter
4. Earth Observation / Space Station / Constellation – Seven years, low earth orbit

Typically, telecommunications processors have the most stringent design requirements. Not only are they required to operate for up to 17 years in a geosynchronous orbit, but they also require high availability due to their commercial application. It is therefore this class of mission we will focus upon.

Radiation Effects

Radiation effects fall into four types: Total Ionizing Dose (TID), Total Non-Ionizing Dose (TNID), Single-Event Effects (SEE) and Deep Dielectric Discharge (DDD). The first three of these categories have the potential to affect electronic components while the fourth, Deep Dielectric Discharge, affects the overall system by allowing a buildup of charge in materials leading to an electrostatic discharge, potentially damaging components.

Both types of total-dose radiation—ionizing and non-ionizing—are long-term effects upon electronic components which result in the degradation of component parameters over time. One especially problematic aspect of Total Ionizing Dose is Enhanced Low-Dose Rate Sensitivity. ELDRS occurs when a device (typically bipolar or BiCMOS) has experienced a dose of radiation at a lower dose rate over a longer period of time. The overall dose might be the same as if the radiation had occurred at a higher dose rate, but with ELDRS the parametric degradation will be worse.

Single-Event Effects are different than total-dose radiation, being instantaneous and therefore occurring at any point within the mission. These effects can be either destructive or nondestructive. Table one below lists the different types of SEEs and their resultant effects.

Description		Effect	Device /Technology Affected	Destructive
Latchup	SEL	High Current Conditions	CMOS, BICMOS	Yes
Snapback	SESB	High Current Conditions	N Channel MOSFET SOI devices	Yes
Gate Rupture	SECR	Rupture of gate dielectric	Power MOSFET	Yes
Hard Error	SHE	Unalterable change of state in a memory element	Memories, latches, Registers	Yes
Burn Out	SEB	Destructive burn out due to high current conditions	BJT, N Channel Power MOSFET	Yes
Upset	SEU	Corruption of Register / Memory eleclment	Memories, latches, Registers	No
Multipe Bit Upset	MBU	As per SEU but multiple bits effected	Memories, latches, Registers	No
Functional Interrupt	SEFI	Loss of normal operation	Complex device with built in state / control e.g. FPGA	No
Transient	SET	Impulse response	Analogue and mixed signal circuits	No
Disturb	SED	Momentary corruption of the information stored in a bit	Combinatorial logic	No

Table One. Single-event effects

When designing an FPGA for flight applications, engineers typically tend to focus upon the nondestructive events, such as single-event upsets and single-event functional interrupts, having worked with parts engineers to ensure the devices selected are immune to the destructive effects.

Radiation	Galactic Heavy Ions	Solar Flare Heavy Ions	Solar Flare Protons	Trapped Protons	Trapped Electrons	Gamma Photons
Launcher	x	x	x	x		
	0.1 - 100 MeV.cm^2/mg		0.1 - 500 MeV			
Telecoms	x	x	x	x	x	x
	0.1 - 100 MeV.cm^2/mg		0.1 - 500 MeV		10KeV - 10MeV	
Observation	x	x	x	x	x	x
	0.1 - 100 MeV.cm^2/mg		0.1 - 500 MeV		0.01 - 10 MeV	
Interplanetary	x	x	x			
	0.1 - 100 MeV.cm^2/mg		0.1 - 200 MeV			

Table Two. Radiation requirements by mission type

It is worth noting here that it is not only electronic components but also materials which will be affected by radiation. For example, organic material becomes brittle with radiation exposure.

Where do these effects come from?

Radiation comes from either our own sun or from a source outside our galaxy, for instance supernova 1987A. Radiation can therefore be grouped into one of three sources: solar particles, galactic cosmic rays or trapped particles. It is made up of electrons, protons, heavy ions, UV rays (which mainly affect materials) and neutrons. The composition of the radiation will differ depending on its origin.

- Galactic cosmic rays – 85% protons, 14% alpha and 1% heavy ion
- Solar particles – Ejected during a solar flare event; typically all protons
- Trapped particles – Particles trapped in the earth's radiation belts

Naturally, different mission profiles will be exposed to one or more of these radiation types depending upon the orbit.

Thermal Environment

When many people think of space, they think of the very cold temperatures. However, for the payload engineering team, the thermal challenge faced most often is ensuring that components stay within their derated junction / operating temperature range.

This is especially the case for high-performance FPGAs like the Virtex-5QV, which can require high currents when performing high-end DSP applications. The only thermal path available to remove the heat from the FPGA is via conduction away to the frame and hence the baseplate. This in turn will affect the thermal design of the overall payload system and its location upon the satellite, as most satellite bus providers place limitation on the thermal density of a module on a satellite panel.

The equipment and hence the FPGA will be required to work across a wide temperature range, both during operation and in the qualification campaign. As it is typical for spacecraft bus manufacturers to specify three temperature ranges, the system must operate across all of them in addition to meeting a cold-start requirement.

- Operating temperature - Normal operating temperature in orbit, for example 20 to 50C
- Acceptance temperature – Operating temperature + 5C. This is the temperature at which the design analysis should be performed, for example the Part Stress Analysis, etc.
- Qualification temperature – Operating temperature +10C. This is the temperature the unit will be subjected to during the qualification campaign in thermal vacuum testing.

Subjecting the unit to thermal vacuum testing will result in a higher temperature rise in components than standard atmospheric temperature tests by between 10 and 20C, depending upon the dissipation of the device [01]. This difference will affect the timing performance of the FPGA. It is therefore critical to ensure your design analysis provides sufficient derating and margin.

Vibration and Shock

The main vibration and shock environments occur, not surprisingly, during launch, payload separation and the releasing of solar panels and antenna reflectors, etc. Therefore, the vibration and shock will occur early in the mission life and will vary depending upon the launcher used. It is common at launch that only the key satellite platform systems will be powered; much of the payload will be powered down and then gradually brought to life during the Launch and Early Operations Phase (LEOP).

It is therefore important for the engineering team to know whether the equipment is to be powered during launch or not, as this will make large difference to the design of the system. For instance, if the device is to be powered on during launch, can anything cause glitches that might affect the operation of the system? This kind of problem recently occurred in a piece of equipment where bond wires within a

device were shorting under vibration and causing glitches, which placed the device into an unrecoverable state.

As it is often late in a project when the vibration and shock are tested as part of the qualification programme, the cost of rectifying failures increases dramatically. It is therefore common in space programmes to develop structural models that mount the critical devices in the correct positions on representative cards. However, to reduce the costs of this development, daisychain devices are available. These are identical in packaging and weight, but they allow a simple test circuit to be constructed which allows monitoring for joint failures, momentary glitches or open circuits. This kind of testing therefore can be conducted early in the development phase to reduce the risk.

FPGA Mitigation Techniques

Within an FPGA the engineer must consider several factors:

1. Parametric changes in timing as the device gets slower due to TID
2. SEU bit flips within the design affecting RAM contents, state machines, counters or other design elements
3. SEFI (if applicable), corrupting the configuration of the device and ensuring it no longer performs as designed

FPGAs are mainly affected by TID as opposed to TNID. This total ionizing dose will gradually change the parameters of the device such as timing performance and power required in the core and I/O banks as the device is subjected to radiation. Reduction of this risk requires several measures, including radiation-hardness assurance, which analyzes the design and orbit to predict the total dose the equipment is likely to see during its lifetime; appropriate part selection; and appropriate derating and timing margin on the timing analysis of the system. Derating means that if the design is being targeted to run at 50 MHz, for example, the design is constrained to ensure the performance can meet 55 MHz, providing a margin.

The major worry of FPGA designers, however, is the single-event upset, which can change the state of a register or RAM element. Depending upon where in the design this happens, the effect may not be noticed—e.g., flipping the LSB of an ADC sample being processed, or a catastrophic lockup of a state machine, causing serious behavioural issues with the payload or, even worse, the platform itself.

To prevent these problems, the engineer has several defensive coding techniques available. The simplest solution is to undertake a Triple Modular Redundancy (TMR) approach and majority vote upon the output. However, this technique can reduce the number of available logic resources within the FPGA and can also reduce the maximum operating frequency. The need for TMR will depend upon whether the device is classified as radiation hard or radiation tolerant. If it is rad tolerant, then you will likely see more SEU-type events, requiring more mitigation techniques.

When considering the implementation of TMR, it is necessary to ensure the three modules are also spaced physically apart within the FPGA. Tools like the Xilinx Isolation Design Flow, originally developed for a single-chip crypto solution, can be used to ensure physical separation within the device. The Xilinx TMR tool will also help the designer implement a TMR architecture within the design.

State machines need to be designed to ensure that there are no unused states into which an SEU can place the state machine—that is, an unrecoverable state.

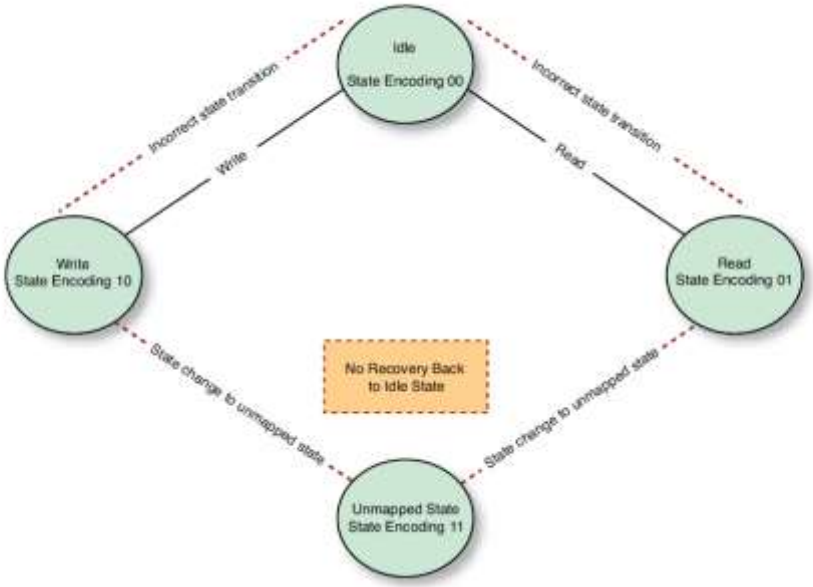

Figure One. Unrecoverable states in a state machine

The engineer has several approaches that can be undertaken to ensure the state machine is safe, as demonstrated in figure two, below [02].

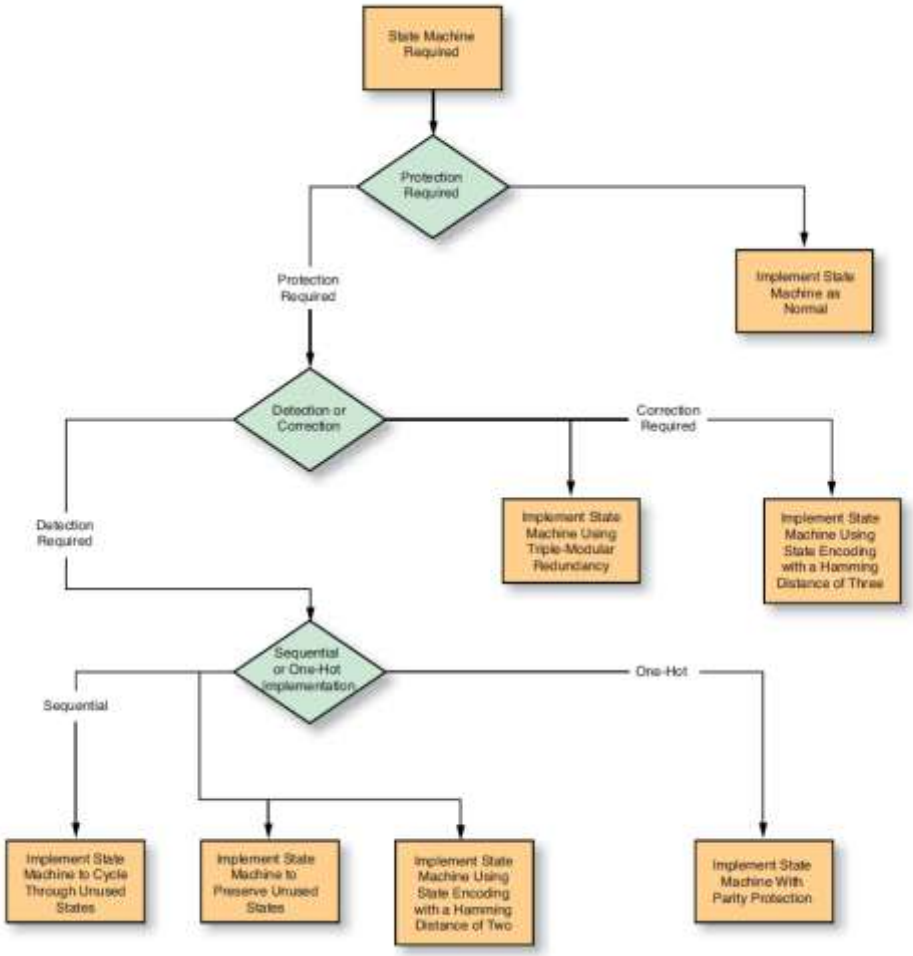

Figure Two. State machine correction / detection schemes

Counters are another area of concern. An SEU close to the terminal count could result in the counter not indicating it has reached its terminal count and restarting. This possibility can be addressed by testing for greater-than or equal-to the terminal value, as opposed to just testing for equality.

Error-detecting and correcting code (EDAC) or error-detection code (EDC) can be used to protect memories and stages of calculations, if desired. This strategy enables the design to identify single-bit errors and correct them, if EDAC has been used, or to identify and report the error, if EDC has been used. Periodic scrubbing of memories is also a useful technique when the memory is not being accessed; the data is read out and has its EDAC checked and, if necessary, corrected before being rewritten to the memory.

At the system level, it is also good practice to store the configuration of the system remotely on a ground station such that disaster recovery is eased if the worst happens and a power-on reset is required.

Many of the challenges the engineer will face in generating a reliable design occur when the synthesis tools remove or optimize the redundancy, or otherwise change the design. One example below, in figure three, shows the potential issues synthesis tools can inadvertently create. Within the original design, Q and !Q cannot be true at the same time. However, in the synthesized code it is possible, and an SEU hit could potentially cause issues by making Q=!Q.

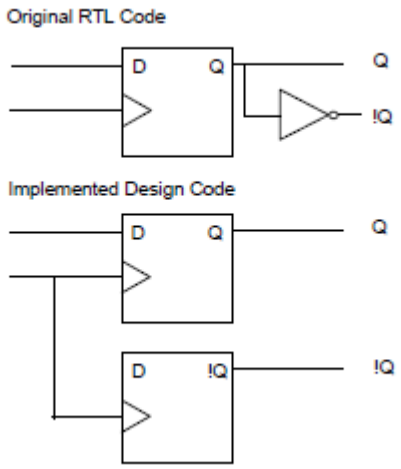

Figure Three. Synthesis optimization issues

Luckily, synthesis tools can be constrained via the tool options and source code attributes. It is often common for an engineer to limit the synthesis tool's ability to replicate logic, pipeline, retime and share resources. Validating that the output of the synthesis tool behaves in the same manner as intended in the RTL is the role of formal equivalence checking. This step will report any mismatch between the performance of the synthesis output and the RTL. The engineer is then responsible for ensuring any optimizations are acceptable or preventing them from happening.

FPGA Choice

Selecting the correct FPGA for the mission is key in spaceflight projects, just as it is on earth-based applications. The selection will be driven by the performance required, operating frequency, special resources (e.g., DSP blocks), high-speed serial links, pin count and configuration architecture. However, the engineer must also consider the

qualification level (QML V), total-dose rating and SEU threshold level. Normally there will be a specialist parts engineer working alongside the hardware engineer to ensure the selected device meets all the requirements for the flight mission. Two commonly used TID and SEU criteria are a TID of at least 100K rad and an SEU immunity of ideally greater than 60 Mev.cm^2/mg, as above this rate no further SEU analysis is needed. However, not all flight FPGAs are specified above this rate.

SEE Theshold MeV.cm2/mg	Analysis Requirement
>60	SEE Risk negilgible
15 <LET < 60	SEE Risk, heavy ion induced SEE rates to be analysed
LET < 15	SEE Risk high, heavy ion and proton induced SEE rates to be analysed

Table Three. SEU testing-level requirements

The major choice between FPGA families is in the reprogrammable versus one-time programmable technologies. The reprogrammable technologies will require additional external configuration memory and mitigation for the configuration suffering from a single-event functional interrupt, which changes the behaviour of the FPGA. Depending upon the mission type, this mitigation could be as simple as reconfiguring the device before each operation on a science mission or implementing readback and correction of the FPGA configuration data using either the same FPGA or a monitoring device. However, reconfigurable FPGAs allow for design changes much later in the development cycle or potentially even in orbit if required.

One-time programmable devices are live at power-on, and there is no chance of a SEFI affecting the configuration of the device. Use of these devices reduces the supporting circuitry needed within the hardware design.

Supporting Technology

It is not just the FPGA that must be designed such that it will perform as desired in space. The overall system must also be able to function within the operating environment, and this includes the supporting hardware. Of main importance is the power supply for the FPGA, which will often be required to provide a high current at low voltage. These devices may also be subject to SEE events, which will affect the output voltage. It is critical to ensure this disturbance to the output rail does not stress or damage the FPGA. For instance, one commonly used POL devices can output a glitch of up to +0.9V on the output rail [03].

The JTAG Test Access Port of the FPGA must also be protected, as an SEU hitting the TAP could result in undefined behaviour of the FPGA. The most common method of protecting the TAP this is to hard-tie the Trst (TAP reset) pin to its asserted state, holding the TAP controller in permanent reset during flight [04]. Unfortunately, not all devices implement this optional TAP pin. If this is the case, then the best mitigation strategy is to clock the TCLK from an independent source (not FPGA generated, otherwise the potential for deadlock occurs) and hold the TMS high. This will, if the worst-case scenario occurs, ensure the TAP controller cycles back to its reset state. However, depending upon the effect, a power-on-reset may be required.

Adding filtering will protect reset circuits to the FPGA from Single Event Transients SET causing inadvertent reset. It is also important that reset be correctly handled within the FPGA and synchronized correctly to ensure that no metastability event can be caused by the reset removal too close to a clock edge.

Conclusion

FPGAs will continue to be used in many challenging environments such as spaceflight. The techniques and approaches presented above will enable the FPGA, hardware and systems designers to design safe and reliable FPGAs and systems for this and other harsh environments.

References

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