Space: The Final Frontier – FPGAs for Space and Harsh Environments

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FPGAs offer several benefits to the system designer:

- Flexibility of Design – performance, upgrades
- Reduction in NRE and Cost.
- Reliability – One Device as opposed to lots if using discrete devices.
- Time to market can be reduced.
- Maintainability – ability with some FPGA to update in the field.
It therefore follows that FPGAs will be used in harsh and demanding environments and we want these to work correctly and safely.

When we use an FPGA in a space mission we need to consider three main factor besides the functionality.

- Radiation
- Thermal Environment
- Dynamic Environment
Each space flight mission will change to what degree these need to be considered

1. Launcher – Lifetime less than 20,000 seconds
2. Telecommunications – 17 Years GEO
3. Science – 7 Years Interplanetary mission
4. Earth Observation – 7 Years LEO

Telecommunication missions are seen as having the most stringent design requirements. Not only do they have to operate for up to 17 years but also require a high availability due to their commercial application. We will therefore focus upon these missions today.
Introduction 4
Radiation Effects

Radiation falls into four types

- Total Ionizing Dose (TID)
- Total Non Ionizing Dose (TNID)
- Single Event Effect (SEE)
- Deep Dielectric Discharge (DDD)

The first three of these categories have the potential to effect electronic components while the fourth DDD is a more systematic effect.

DDD allows a build up of charge in materials leading to an electrostatic discharge potentially leading to damage, for this reason all floating metal must be connected to ground.
Both TID and TNID are long term effects upon electronic components which result in the degradation of component parameters over time, for example Timing or Power parameters.

One problematic aspect of TID is Enhanced Low Dose Rate Sensitivity (ELDRS).

ELDRS – Is when a device experiences worse performance degradation when subjected to a lower dose rate. This normally effects Bipolar or BiCMOS technologies.
Single Event Effects are different to total dose radiation being instantaneous and therefore occurring at any point within a mission.

SEE can be either destructive or non-destructive.

When designing an FPGA for a flight mission engineers tend to focus upon the non-destructive effects. This is due to having worked with part and radiation engineers to ensure the parts selected are radiation hard in line with the radiation hardness assurance requirements.
## Radiation Effects 4

<table>
<thead>
<tr>
<th>Description</th>
<th>Effect</th>
<th>Device / Technology Affected</th>
<th>Destructive</th>
</tr>
</thead>
<tbody>
<tr>
<td>Latchup</td>
<td>SEL</td>
<td>High Current Conditions</td>
<td>CMOS, BICMOS</td>
</tr>
<tr>
<td>Snapback</td>
<td>SESB</td>
<td>High Current Conditions</td>
<td>N Channel MOSFET, SOI devices</td>
</tr>
<tr>
<td>Gate Rupture</td>
<td>SECR</td>
<td>Rupture of gate dielectric</td>
<td>Power MOSFET</td>
</tr>
<tr>
<td>Hard Error</td>
<td>SHE</td>
<td>Unalterable change of state in a memory element</td>
<td>Memories, latches, Registers</td>
</tr>
<tr>
<td>Burn Out</td>
<td>SEB</td>
<td>Destructive burn out due to high current conditions</td>
<td>BJT, N Channel Power MOSFET</td>
</tr>
<tr>
<td>Upset</td>
<td>SEU</td>
<td>Corruption of Register / Memory element</td>
<td>Memories, latches, Registers</td>
</tr>
<tr>
<td>Multiple Bit Upset</td>
<td>MBU</td>
<td>As per SEU but multiple bits affected</td>
<td>Memories, latches, Registers</td>
</tr>
<tr>
<td>Functional Interrupt</td>
<td>SEFI</td>
<td>Loss of normal operation</td>
<td>Complex device with built in state / control e.g. FPGA</td>
</tr>
<tr>
<td>Transient</td>
<td>SET</td>
<td>Impulse response</td>
<td>Analogue and mixed signal circuits</td>
</tr>
<tr>
<td>Disturb</td>
<td>SED</td>
<td>Momentary corruption of the information stored in a bit</td>
<td>Combinatorial logic</td>
</tr>
</tbody>
</table>
While we are focusing upon the effects on electronic components it is worth noting that radiation also effects other materials within the design.

Radiation Requirements by mission Type
Where do these effects come from?

Radiation comes from either our own sun or from a source outside of our galaxy.

Radiation can therefore be grouped into one of three sources:

- **Solar Particles** – Ejected during a solar flare event
- **Galactic Cosmic Rays** – High Energy charged particles e.g. Supernova 1987A
- **Trapped Particles** – Particles trapped in the Earth's radiation belts

Radiation consists of Electrons, Protons, Heavy Ions, UV Ray and Neutrons.
Typically many people think of the cold temperatures of space however, for the payload engineering team the thermal challenge faced most often is ensuring components and equipments stay within their derated junction / operating temperature range.

This is especially the case for high performance FPGA’s like the Virtex 5QV which can require high currents when performing high end DSP applications.

- How can we address this and ensure the FPGA stays within the derated junction temperature range?

- Why do we have a derated junction temperature range?

Most satellite bus providers place limitations on the thermal density of the module on the satellite panels.
Both the equipment and FPGA will be required to operate across wide temperature ranges. It is typical for your design to have to meet three operating temperature ranges and still operate.

- Operating Temperature, the normal operating temperature in orbit (-20°C to 60°C) Applicable to all units
- Acceptance Temperature, this is the temperature at which the design analysis should be conducted this is normally operating temperature +/- 5°C
- Qualification Temperature, this is the temperature the unit has to operate at during qualification normally operating temperature +/- 10°C

These temperatures will depend upon the spacecraft bus your payload is flying on.
Performance in the thermal environment is tested during thermal vacuum testing (TVAC)

Why TVAC? A higher temperature rise will be exhibited in components than standard thermal testing by between 10 and 20C.

This can have a significant effect upon both the power required and the timing performance of your design.
Dynamic Environment

The main shock and vibration environments occur during

- Launch
- Payload Separation from the launcher
- Extension of solar panels
- Extension of antenna reflectors

Depending upon the role of your equipment e.g. platform or payload it will be either unpowered or powered during launch. It is mainly platform subsystems which are powered during launch and therefore must operate correctly through out launch. Unpowered equipment must be capable of operating post exposure to the dynamic environment.
An example the vibration profile can cause, we recently had issues with an equipment a subcontractor supplied. Upon further investigation it was found vibration was causing bond wires within a FPGA to cause glitches and result in a un recoverable state.

Often it is late in a project when the qualification is undertaken hence the cost of failures can be significant not only financially but also effecting launch dates.

How can we de risk this?
Dynamic Environment 3

Development of a structural model early in the programme which is representative of the final design.

Daisy chain devices can be purchased from many component suppliers in the same packaging which allows you to monitor the package mounting to ensure it can survive or operate within the dynamic environment.

While this can be tested early it is by no means cheap, but it is cheaper than finding out during the qualification programme.
Model Philosophy

Developing equipment for a satellite will require a number of models being developed prior to delivery of the final flight models.

- Engineering Model, the initial design representative in size and function to the final version by may use commercial parts
- Engineering Qualification Model, the model subjected to the qualification campaign. This usually includes design updates from the EM and uses identical components to flight however, they do not need to be screened to flight standard
- Proto Flight Model, A flight model subjected to the same qualification levels as the EQM. Sometimes for cost issues this is also flown
- Flight Model, the models actually flying these are tested to acceptance level testing.
Model Philosophy 2

This model philosophy will effect the choice of FPGA used

– Engineering Model, FPGA design is likely to change often so either a socketed device (if final device is one time programmable) or commercial reprogrammable device is used. Most suppliers of space grade components offer a low cost prototype solution.

– Engineering Qualification Model, the FPGA should be a representative of the flight version in every way although it may be screened to a lower level e.g. Xilinx B Flow or RTAX Proto

– Flight Model, the final FPGA screened to the required levels needed for the mission.
FPGA Mitigation Techniques

Within an FPGA the engineer must consider several factors

- Parametric changes in timing as the device gets slower
- SEU bit flips within the design affecting RAM contents, state machines, counters and other functions.

• SEFI (if applicable) corrupting the configuration of the device and ensuring it no longer performs as designed.
FPGA Mitigation Techniques 2

FPGA are mainly affected by TID as opposed to TNID, TID will gradually change the parameters of the FPGA such as timing performance and power required.

Usually the development tools include the data to include these parametric changes.

For example timing analysis should take into account the effects of the parametric changes.

This is where your radiation hardness assurance comes into play ensuring the component selected are suitable for the mission.

However many companies also ensure derating is included within the timing constraints. E.g. if you are designing to operate at 50 MHz your constraints should be set for 55 MHz providing a margin.
The major worry of the FPGA designer is the single event upset. Depending upon where in the device this happens the effect may or may not be noticed, for example

- Flipping the least significant bit of a ADC digitised output, this will quickly clear as other samples are clocked through and will have a similar effect as a rounding error when further processed.

- Flipping a state bit on a state machine and causing the state machine to enter a unused state and hence locking up the machine. This could result in catastrophic loss of the mission.

But it is not just state machines, counter, RAMs any stored value can be flipped
The Unmapped State Machine

- **Idle**
  - State Encoding 00
  - Incorrect state transition
  - Read

- **Write**
  - State Encoding 10
  - Incorrect state transition
  - Write

- **Read**
  - State Encoding 01
  - Incorrect state transition
  - Read

- **Unmapped State**
  - State Encoding 11
  - State change to unmapped state

**No Recovery Back to Idle State**
FPGA Mitigation Techniques

How can we harden state machines?
Triple Modular Redundancy – Instantiate three implementations of the state machine and majority vote on the output. This obviously has an area penalty and can reduce the operating frequency. There are tools like XMR from Xilinx which will assist with inserting TMR.

TMR also requires that the instantiations are separated physically from each other to ensure more than one instantiation cannot be effected by a SEU and create a MBU.

What other options are available?
FPGA Mitigation Techniques 6

State machine choices other than TMR

- State Machine Required
- Protection Required
  - Protection Required
    - Detection or Correction
      - Detection Required
        - Sequential or One-Hot Implementation
          - Sequential
          - Implement State Machine to Cycle Through Unused States
          - Implement State Machine to Preserve Unused States
      - Correction Required
        - Implement State Machine Using Triple-Modular Redundancy
        - Implement State Machine Using State Encoding with a Hamming Distance of Three
    - One-Hot
      - Implement State Machine With Parity Protection
  - Implement State Machine as Normal
RAMS can be protected by error protection codes. Depending upon the device these are hard coded into the RAMS and transparent to the user or require user implementation.

Regardless of how they are implemented it is a good idea to use a scrubbing algorithm which will read back contents out of the memory periodically and ensure correction of any errors to prevent a build up of errors.

If these RAMS are being used to store the configuration of the system it is a good idea to have a copy of this configuration on the ground payload control system to ease recovery in the worse case.
One of the challenges in ensuring your design will be suitable for space flight is will come when you are synthesising the system. For example
If you are using a SRAM based FPGA you need to consider what happens if a SEU hits a configuration bit. This is called a single event functional interrupt in that it could effect the operation of the FPGA.

It is important to note that not all configuration bits will have an impact on the design. In fact the Xilinx tools will report the number of configuration bits that are essential to the design i.e. if they get hit they will effect the design.

This is reported in the bit gen report when the essential bits option is set

“This design has 557763 essential bits out of 16028176 total (3.48%).”
How can we mitigate this in flight (and in other applications like aerospace)

Easiest is reconfigure the device at periodic times to clear any SEFI effects. This is easier on science missions than on telecoms processors where dropping links costs money.

If that is not possible then Xilinx devices from the Spartan 3A onwards have an inbuilt CRC checker. This reads back the configuration data following initial configuration and calculates a CRC. It then continues to read back the configuration and checks the CRC is the same as the initial one.

This is a broad brush and check the entire device configuration and not just the essential bits. Enabled in the constraints file.

For aerospace devices there are more advanced solutions based around the Soft Error Mitigation IP which can monitor changes to the essential bits.
FPGA Choice

Selecting FPGA depends upon mission ad is driven buy performance requirements, special resources and configuration architecture.

The device also needs to align with your EEE parts and radiation assurance plans which will call up qualification level (QML V) total dose rating and SEU threshold

Two commonly used criteria are TID and SEU performance, a TID of at least 100 K Rad and a SEU immunity of greater than 60 Mev.cm²/mg however not all devices may meet this.
SEE analysis requirements

<table>
<thead>
<tr>
<th>SEE Threshold MeV.cm²/mg</th>
<th>Analysis Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt;60</td>
<td>SEE Risk negligible</td>
</tr>
<tr>
<td>15 &lt; LET &lt; 60</td>
<td>SEE Risk, heavy ion induced, SEE rates to be analysed</td>
</tr>
<tr>
<td>LET &lt; 15</td>
<td>SEE Risk high, heavy ion and proton induced, SEE rates to be analysed</td>
</tr>
</tbody>
</table>

FPGA SEU rates are often given as upsets/device-day as calculated by tools like CREME96.
This can be used to determine days between events.
The major choice between FPGA missions for flight is reprogrammable vs one time programmable.

OTP – Has no issues with configuration being effected by SEFI but typically lower performance and hard to change later in development.

Reprogrammable – Split into SRAM and FLASH based need to consider SEFI on the configuration memory.

Flash based devices – LEO only and not re programmed in flight
Supporting Technology

It is not just the FPGA which needs to be designed such that it will perform as desired but the entire system.

Of critical importance to the FPGA are obviously the power supplies, Oscillators, Resets JTAG Test Access Port.

Power supplies – Experience output rail disturbances, need to ensure these disturbances do not damage or stress the FPGA.

Oscillators – Experience missing pulses

Reset – SET causing inadvertent reset

JTAG TAP – If not held in reset a SEU could effect the TAP State Machine and result in undefined behaviour of the FPGA.
Supporting Technology 2
The End

Thank you for your attention

Questions?

I will be talking more about system design issues and challenges tomorrow

Flying High Performance FPGA's on Satellites
Two Different Case Studies