designwest

center of the engineering universe

Flying High-Performance FPGAs on Satellites:
Two Case Studies

April 22-25, 2013
McEnery Convention Center
San Jose, CA
www.ubmdesign.com

Your Company Logo Here

UBM
Tech

Introduction

Often when considering flying a FPGA or other high-performance device the first thoughts might be how will radiation effect the device.

However that is just one of many parameters which must be considered. Here we will look at two very different missions and the challenges faced by both when designing in a high performance FPGA.

- Ukube1, a CubeSat mission scheduled for launch in late 2013
- A generic FPGA processing card for use in a number of GEO missions

What is a High Performance FPGA??

"High-performance FPGAs are those which offer a large number of not only logic resources but also advanced features such as DSP blocks, embedded processors, high-speed serial links (HSSLs), advanced clocking resources and support for a large number of I/Os. Often these devices are reprogrammable."

Common Issues

In both cases, regardless of the mission the engineer responsible for the overall development of the mission will have to address the following:

•Device selection – What is the required function of the device? how many resources are required (RAMS, LUTs, DSP blocks, HSSLs)? how many I/O pins are required? Typically your choice is limited to space-qualified components and approved component lists like the ESA ESCC system or the NASA parts selection list.

• Physical constraints – What are the defined parameters for the PCB size? Are there any constraints on mass? How will the power dissipated within the FPGA be handled?

Common Issues 2

- Reliability – How long is the intended mission life? What is the desired reliability for the mission, and how do we determine the reliability of the design? Is redundancy required?

- Power budget – Are there any limitations on the power that the payload can draw? What voltages are available? Must we protect the satellite bus supplies in the event of a failure?

- PCB technology – What considerations are needed for the actual PCB design? Are there any specific routing rules or stackups required? Is the FPGA mounting method even qualified for the rigours of spaceflight?

UKube

Ukube1 is the first in a series of planned satellites to be launched by the U.K. Space Agency; the Astrium Janus payload was proposed and accepted as a technology demonstrator payload.

This payload has two FPGA-based experiments. The first is based on an Astrium-held patent on the use of cosmic radiation to generate true random numbers, while the second experiment involves the flying of a large, high-performance FPGA.

UKube 2

• CubeSats are a class of nanosatellite scalable from the basic 1U form factor (10cm * 10cm * 10cm) to 3U and beyond.

Main challenges of UKube mission:-

• Power Budget – Sunlight average 400 mW.

• Physical constraints – Limited to 310g for the payload PC104 sized, with a height restriction of 35 mm.

• Device selection – Flight-grade components are expensive and need to be selected such that they will allow the power budget to be achieved.

UKube 3

The power architecture of the UKube1 provides three regulated rails to each payload at 3.3V, 5V and 12V, with a maximum acceptable current of 600 mA to be drawn from any one of these supplies.

However in orbit average has to remain @ 400 mW.

Achieving the power budget is one of the major challenges of this mission.

UKube 4

The architecture developed for the Janus payload was based around two FPGAs

1.Radiation Hardened One Time Programmable RTAX2000
- Performs the Random Number Experiment (In conjunction with a large SRAM) and monitors the Virtex 4 for SEU & SEFI Events. This device also communicates with the UKube 1 Mission Interface Computer over the I2C bus.

1.Radiation Tolerant Xilinx XQR4VSX55
- Subject of the second experiment to determine performance in a space environment - essentially SEU / SEFI hunting

UKube 5
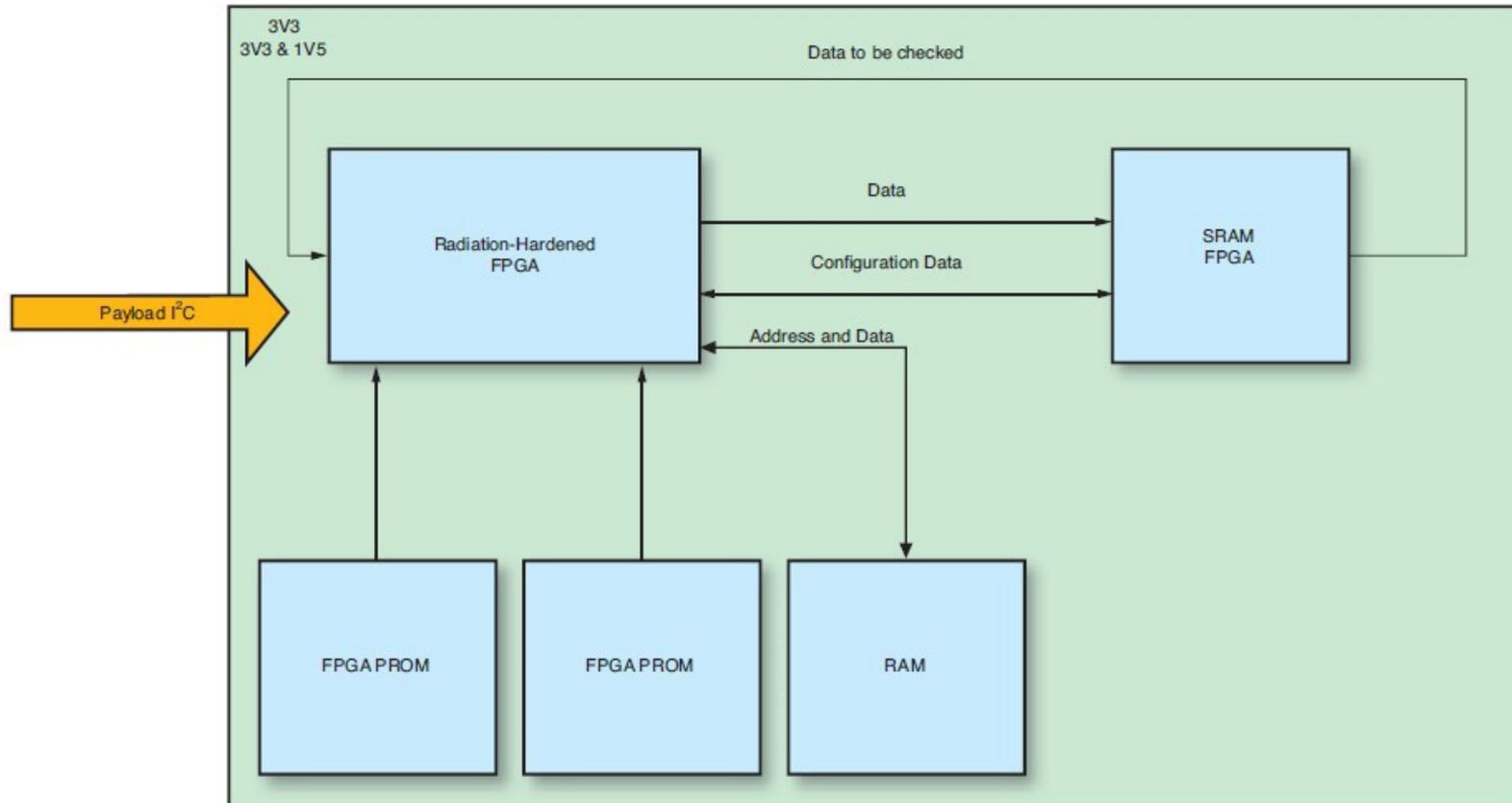
UKube 6

The power architecture of the design was complicated by not only the power and current limits, but also by the number of voltage rails required

- First experiment requires 1v5 and 3v3
- Second experiment requires 1v2, 2v5, 3v3 and 1v8

The next step was to determine the power required allowing the sizing of power supplies. This was achieved initially using spreadsheets provided by the FPGA manufacturers.

After this analysis it was determined to have two modes of operation to ensure more flexibility with the run time.
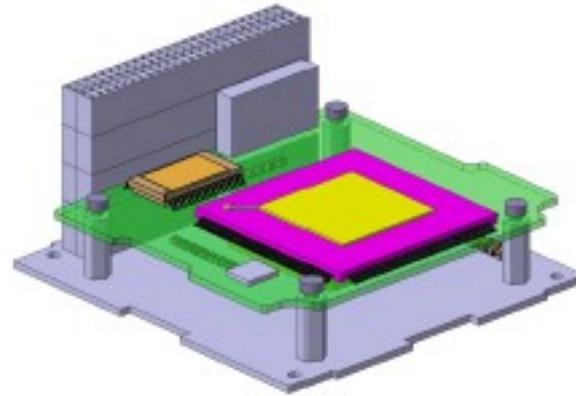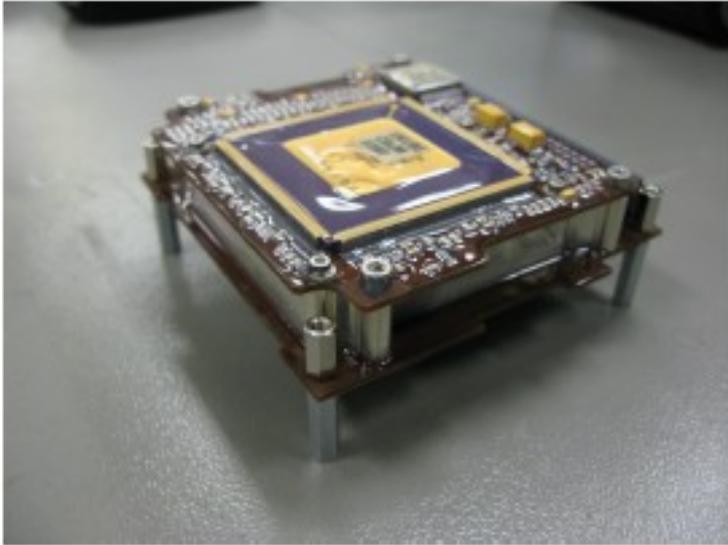
UKube 7

To ensure the power requirements could be met, high-efficiency switching converters were used to minimize losses in the voltage regulation for the FPGAs.

This power estimation was then verified in the lab once the hardware arrived.

UKube 8

FPGA Processing Solution

Generic processing solution is a Virtex-5QV-based solution with a path to ASIC for specific missions. The processor is designed to perform signal processing on telecoms and earth-observation missions; therefore, flexibility of the design is key.

The idea behind the generic processing system is to enable a single design to be reused for a number of missions. Most of these missions will require a high-performance FPGA to implement the mission processing requirements

FPGA Processing Solution 2

The three most challenging aspects of this design are:

- Physical constraints – The high power dissipation involved with using a high-performance FPGA or ASIC presents challenges.

- Reliability – While redundancy would be implemented at a module level, with a mission life of 17 years, the failure rate (FIT) of the module must be low.

- PCB technology – The Virtex-5QV has 1752 pins on a 1-mm pitch, ensuring both power integrity and signal integrity, and guaranteeing the mounting method can be qualified for flight.

FPGA Processing Solution 3

Physical Constraints:-

Modern FPGA can require some high worse case currents, this high power dissipation then results in problems for the engineering team to meet the de-rated junction temperature.

The ESA derating requirement on logic devices calls for derated junction temperature of 110C or Tj max – 40C, whichever is lower.

This means the Virtex 5QV has a maximum junction temperature of 85C.

FPGA Processing Solution 4

It must achieve this junction temperature at acceptance temperature (5C above the operating temperature).

Ensuring an accurate thermal model will require close cooperation between the FPGA, hardware, PCB and mechanical design teams to accurately determine the power dissipated in the worst case by all of the components. This result can then be subjected along with the PCB placement of components and the mechanical design (showing heat straps, etc.) to thermal modelling in a tool like IDEAS TMG.

FPGA Processing Solution 5

In the quest to reduce the power dissipation of the module, the engineer can:

Look at potential FPGA implementation options to reduce the power, e.g. introducing a pipeline, changing optimization schemes and ensuring dedicated resources are available.

Investigate the power architecture and the losses in conversion. In one recent mission, a change in architecture resulted in a reduction in power losses from 10W to 5W. When considered at a payload level, on a project that contains several modules, this type of savings makes your solution very attractive.

FPGA Processing Solution 6

Reliability:-

Reliability is normally measured in FIT rate or mean time between failures (MTBF). These figures can be used to obtain the overall probability of success for a given mission duration.

For spaceflight missions where redundancy is the only realistic option for repair, it is imperative that the failure rate be as low as possible

To accurately determine the failure rate, you must consider the failure rate of the component interconnections (solder joints), the devices used (hybrid, IC, PCB, etc.) and the operating environment (ground, aircraft, space vehicle, etc.).

FPGA Processing Solution 7

Two basic methods of determining Reliability

•**Parts count:** This technique, which is based around reference stresses on components, involves simply summing the failure rates of the components. The resulting analysis tends to give a more conservative (pessimistic) failure rate.

•**Stressed reliability:** This approach utilizes actual electrical and thermal stress applied to each component to determine a more accurate failure rate for the system.

FPGA Processing Solution 8

To achieve a good reliability (.999) over the mission duration, redundancy will be required.

Redundancy can be either hot or cold spared, redundancy for the generic processor system will be cold spared.

The current parts count analysis for the generic FPGA processing card is 604 FITs, giving a probability of success for a 17-year mission at 0.9141 for a single module, or a reliability of 0.997 when in a 2-for-1 configuration.

FPGA Processing Solution 9

Probability of Success	MTBF	FIT (1e-9 hours)
0.99	14827564	67.44196147
0.95	2905292	344.1994815
0.9	1414400	707.0135747
0.85	916951	1090.570816
0.8	667830	1497.38706
0.75	518009	1930.46839
0.7	417808	2393.443879

FPGA Processing Solution 10

PCB Technology:-

•The first and often most overlooked aspect is actually qualifying the mounting of the component to the device, since without a qualified mounting process the customer PA team will be very unlikely to sign off on the design and manufacturing

•Qualification involves mounting a number of samples to a representative PCB and then subjecting these to a number of thermal cycles before experiencing shock and vibration profiles. This ensures the component will survive the rigours of launch and the mission.
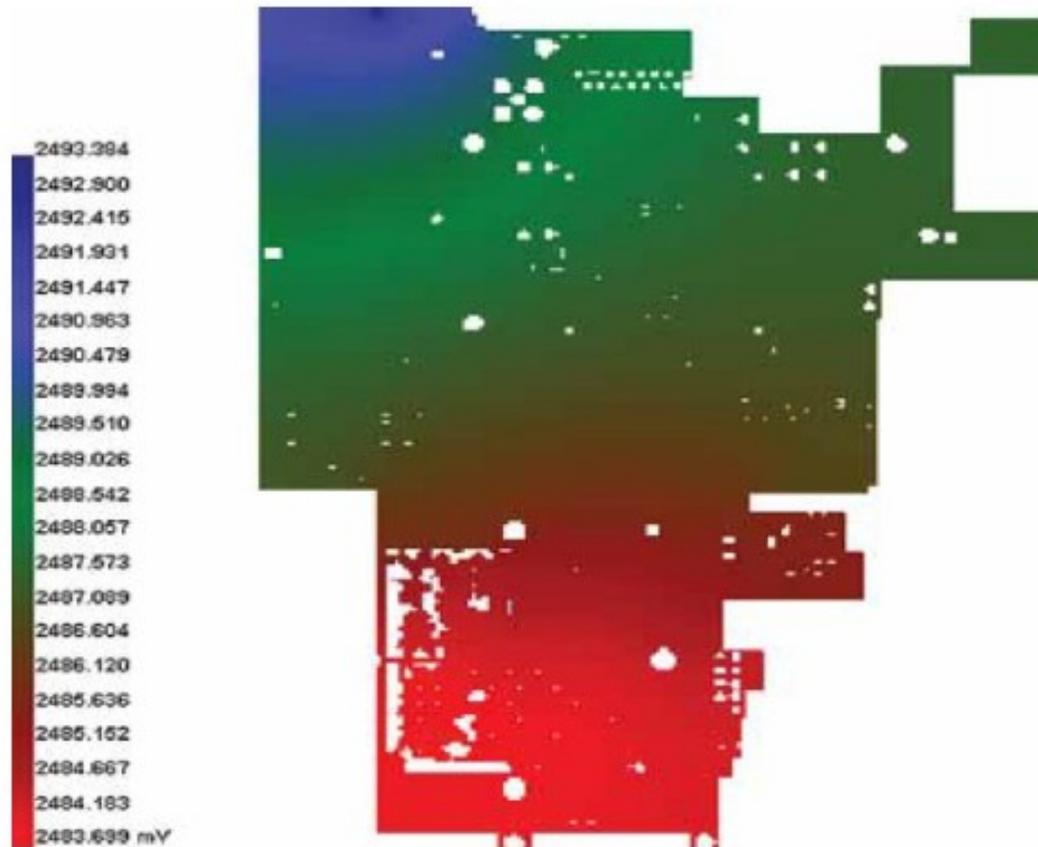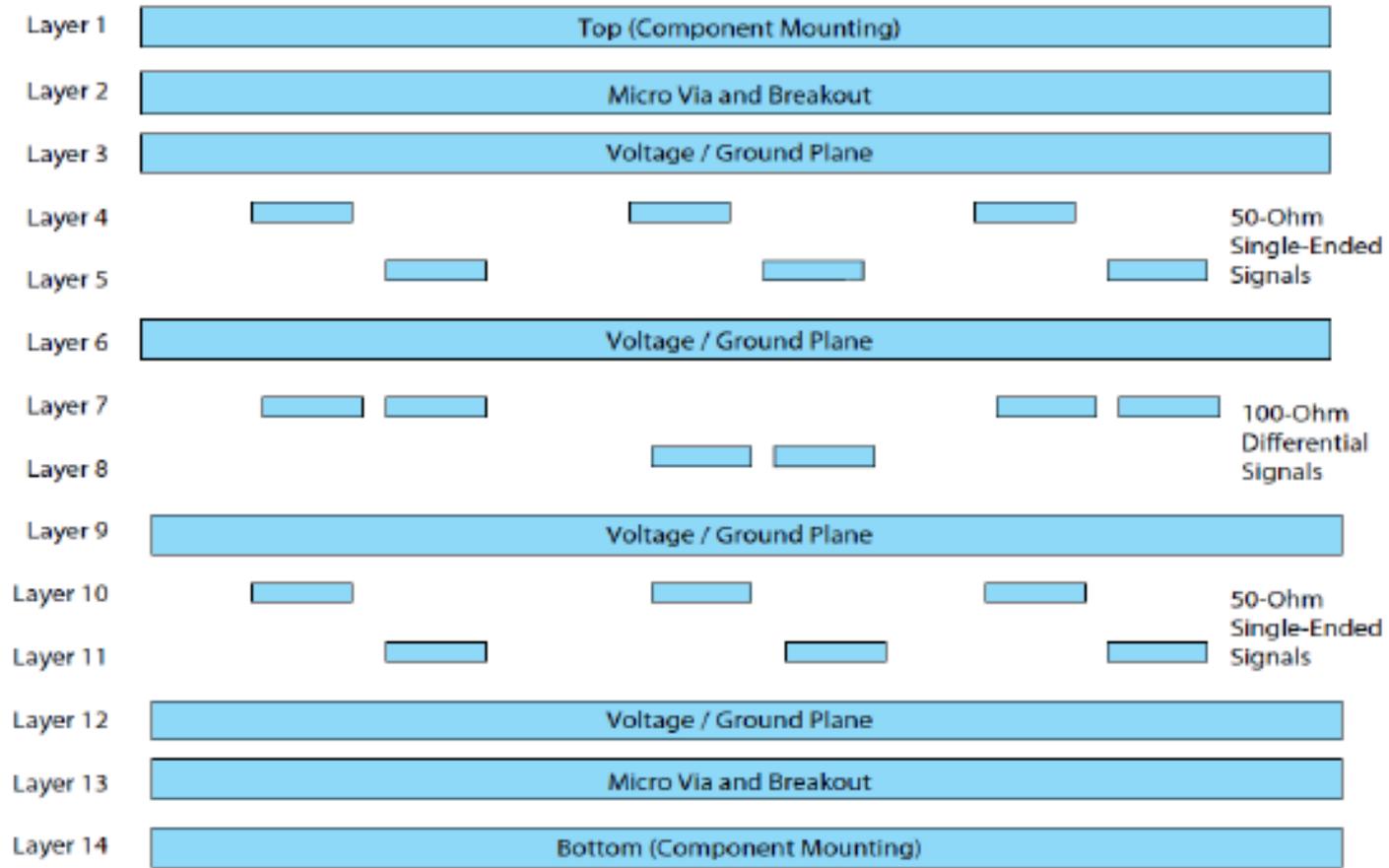
FPGA Processing Solution 11

The high currents required by modern FPGAs can create an interesting challenge in not only ensuring that the power supply can provide the necessary currents at the required low voltages, but also ensuring your PCB design does not exhibit too much voltage drop down the planes, especially when those planes are peppered by 1752 vias.

The generic FPGA processor card is designed to interface using both high-speed serial links at 3.125 GBps and low-voltage differential signaling (LVDS) I/O operating at speeds of up to 400 MHz double data rate. This means the PCB needs to be designed to have the required characteristic impedances.

2493.394	
2492.900	
2492.415	
2491.931	
2491.447	
2490.963	
2490.479	
2489.994	
2489.510	
2489.026	
2488.542	
2488.057	
2487.573	
2487.089	
2486.604	
2486.120	
2485.636	
2485.152	
2484.667	
2484.183	
2483.699 mV	

FPGA Processing Solution 13

Conclusion

There are several major considerations which the design architect must consider.

High performance FPGA offer several benefits to the satellite payloads.