ADIUVO

ENGINEERING AND TRAINING, LTD.

MicroBlaze Booting From QSPI Flash – Via STARTUPE3

Vivado 2020.1

Target Board : KU105

Introduction

Devices in the UltraScale and UltraScale+ range have dedicated pins for QSPI Configuration (UG575) compared to Seven Series (UG475) which mixes dedicated and user IO.

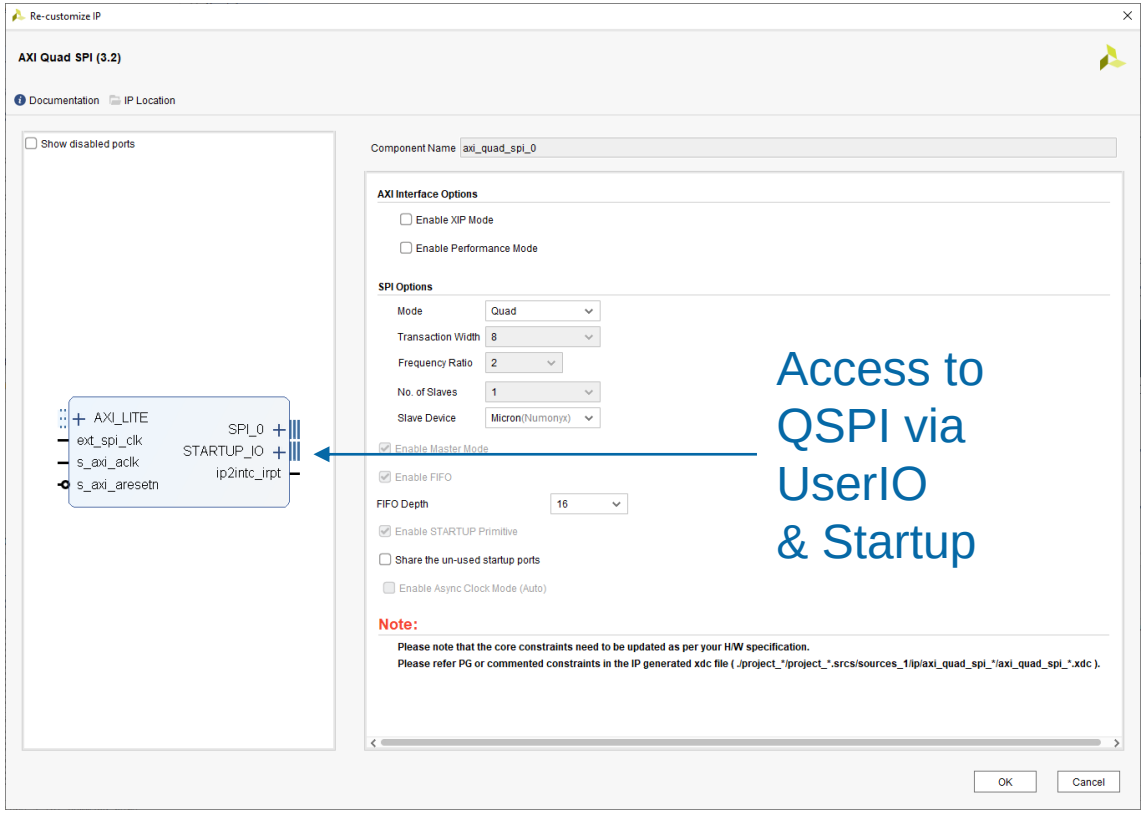
This means post configuration access to the configuration QSPI for software applications using a bootloader is slightly different.

Seven Series – Mix of user IO and Configuration pins

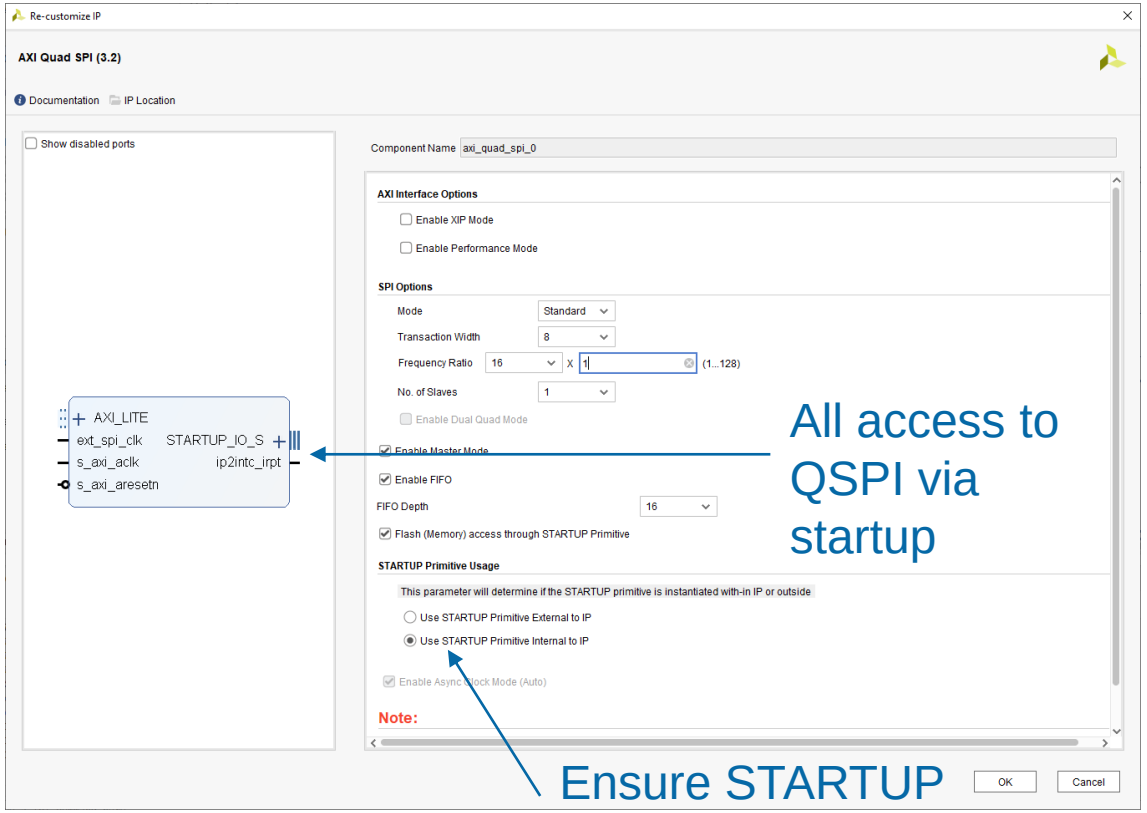
UltraScale / UltraScale+ - Access via configuration pins

© Adiuvo Engineering and Training, Ltd. 2020

Seven Series Difference



Access to QSPI via UserIO & Startup



All access to QSPI via startup

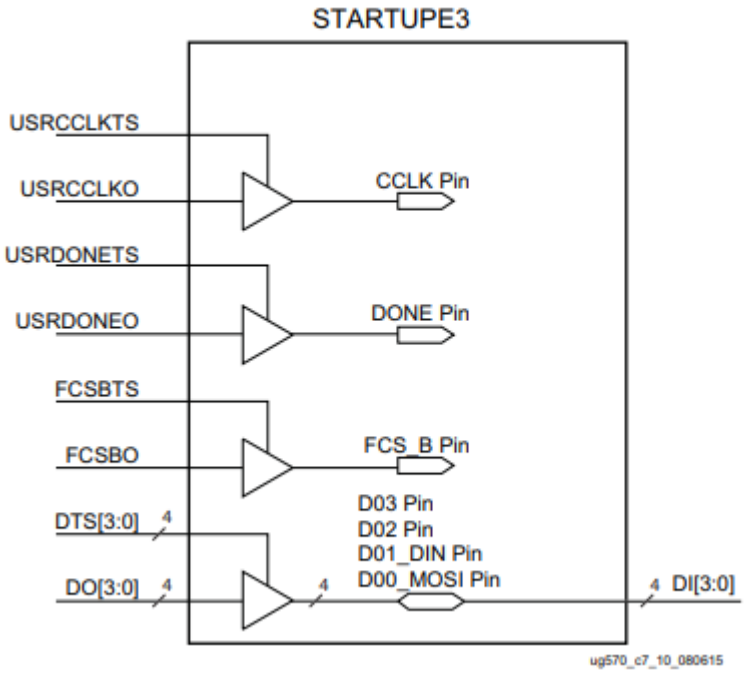
Ensure STARTUP is internal to the IP

© Adiuvo Engineering and Training, Ltd. 2020

STARTUPE3 Concept

Control of dedicated configuration pins allows post-configuration access to the flash. When the flash is only used for configuration the FPGA design does not require the STARTUPE3

STARTUPE3 adds the ability to control the D00-D03 pins and the FCS_B pin. To access the FLASH post Configuration.



© Adiuvo Engineering and Training, Ltd. 2020

STARTUPE3

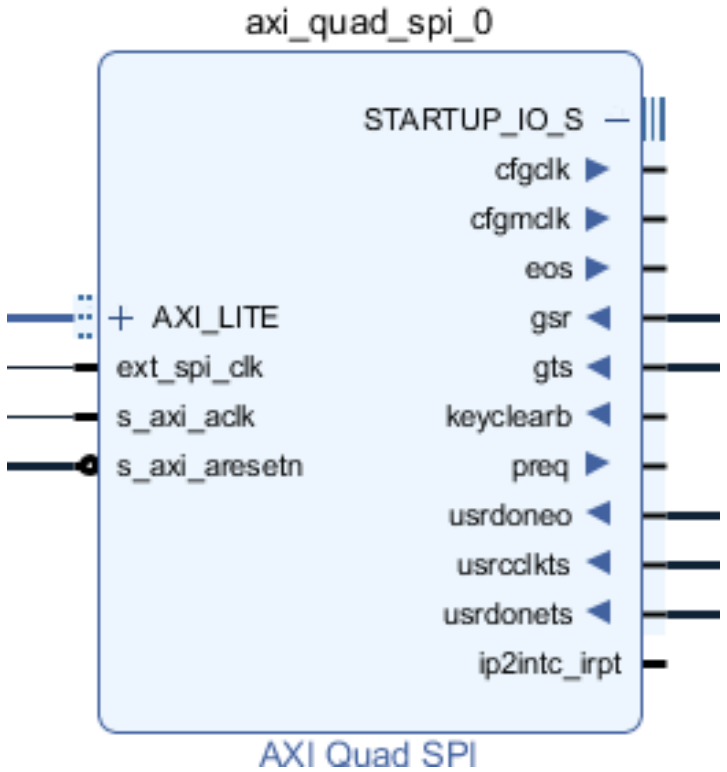
Using the STARTUPE3 will make available several additional configuration pins. Outputs can be ignored but inputs should be addressed.

GSR – Global Set Reset - Tie Low

GST – Global IO Tristate – Tie Low

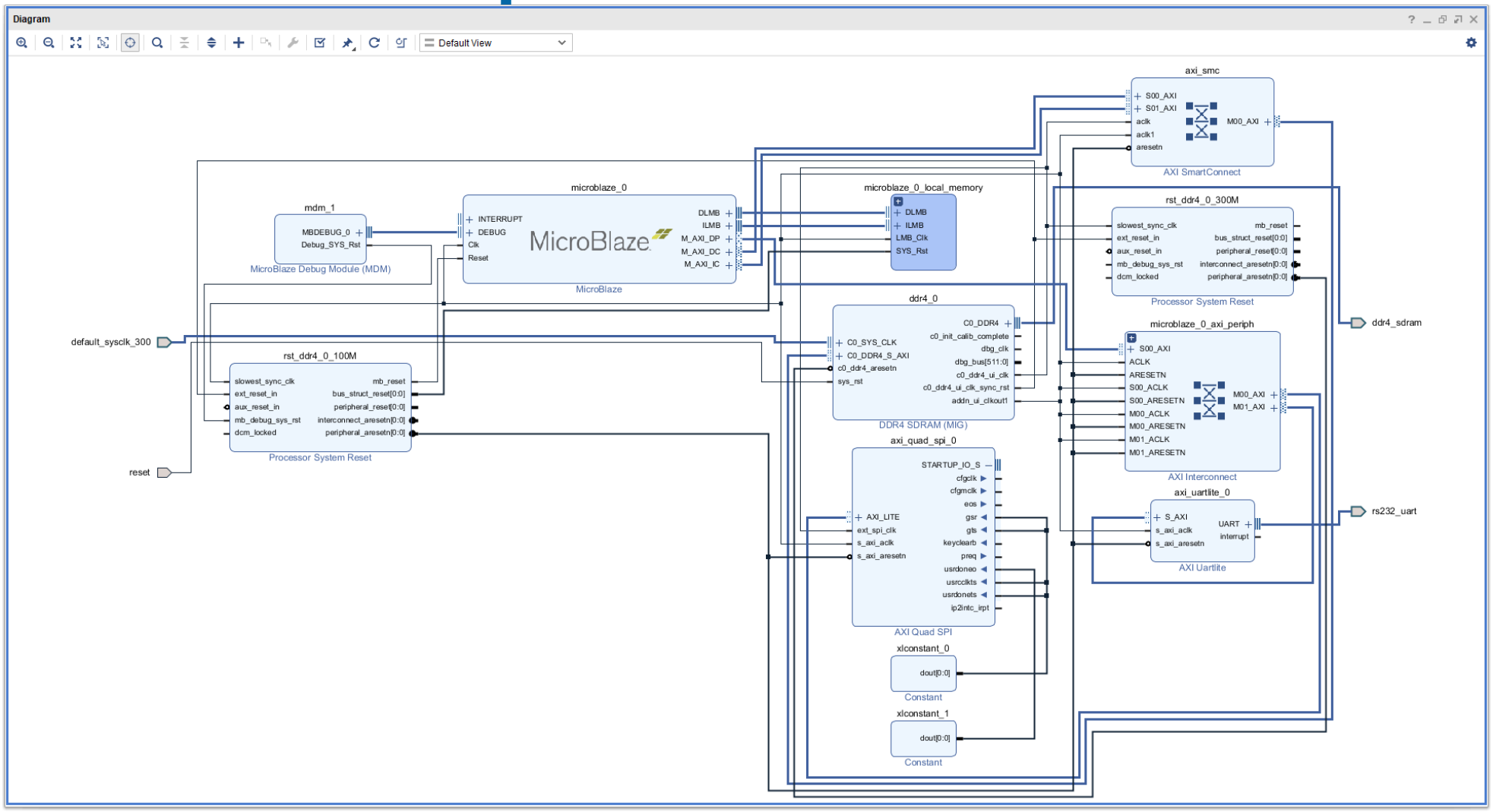
USRCCLKTS – Enable CCL – Tie Low

USRDONETS – User Done – Tie High



© Adiuvo Engineering and Training, Ltd. 2020

KCU105 Example



© Adiuvo Engineering and Training, Ltd. 2020

Software Development

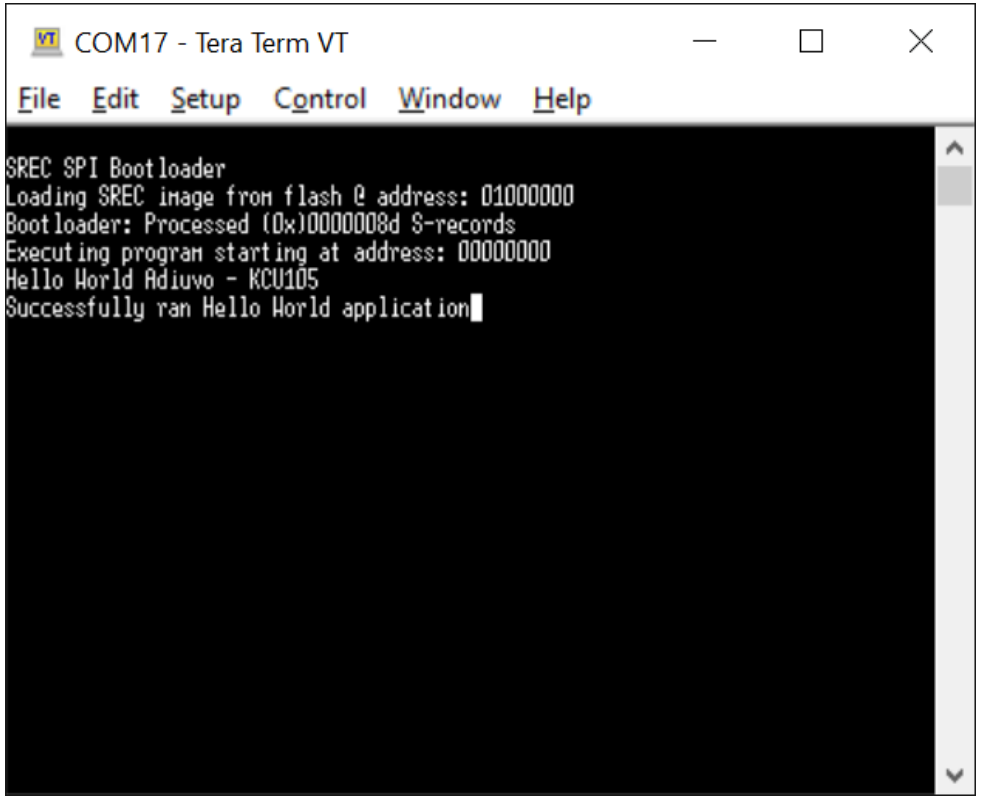
Software Development Flow is identical previous development flow.

Reference Material - User Guides

UG570

UG575

UG475



© Adiuvo Engineering and Training, Ltd. 2020

ADIUVO

ENGINEERING AND TRAINING, LTD.

www.adiuvoengineering.com

adam@adiuvoengineering.com